CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device comprising:

a first plurality of storage circuits to store an upper value;

a second plurality of storage circuits to store a lower value; and

a plurality of compare circuits to determine if a first comparand value is within a range of values defined by the upper value and the lower value.

2. The CAM device of claim 1 wherein the first comparand value is a field of bits within a second comparand value.

3. The CAM device of claim 1 wherein each of the first plurality of storage circuits includes a memory element to store at least one bit of the upper value.

4. The CAM device of claim 1 wherein each of the plurality of compare circuits includes circuitry to compare a bit of the first comparand to a bit of the upper value and to output a result signal in a first state if the bit of the first comparand is greater than the bit of the upper value and to output the result signal in a second state if the bit of the first comparand is less than the bit of the upper value.

5. The CAM device of claim 4 wherein outputting the result signal in a first state comprises switchably coupling a match signal line to a predetermined voltage reference to affect a voltage level of the match signal line.

6. The CAM device of claim 5 wherein outputting the result signal in the second state

comprises decoupling the match signal line from the predetermined voltage reference.

7. The CAM device of claim 5 wherein coupling the match signal line to a predetermined voltage reference comprises coupling the match signal line to a ground voltage reference to pull down the voltage level of the match signal line.

8. The CAM device of claim 4 further comprising a match line, and wherein a most significant compare circuit of the plurality of compare circuits is coupled to the match line, the most significant compare circuit being adapted to affect a logical state of the match line according to the result signal.

9. The CAM device of claim 8 wherein the most significant compare circuit is coupled to output the result signal to the match line.

10. The CAM device of claim 8 wherein at least one other of the plurality of compare circuits is coupled to output the result signal to the most significant compare circuit.

11. The CAM device of claim 1 wherein the upper value comprises a plurality of bits ordered from a most significant bit to a least significant bit, and wherein each of the plurality of compare circuits is adapted to store a respective one of the plurality of bits and to compare the one of the plurality of bits to a respective bit within the first comparand value.

12. The CAM device of claim 11 further comprising a match line and wherein a most significant compare circuit of the plurality of compare circuits is coupled to the match line, the most significant compare circuit including circuitry to affect a logical state of the match line if either (1) a most significant bit of the first comparand value is greater than the most

significant bit of the upper value, or (2) the most significant bit of the first comparand is equal to the most significant bit of the upper value, and a result signal from a less significant compare circuit of the plurality of compare circuits indicates that the first comparand value minus the value represented by the most significant bit of the first comparand value is greater than the upper value minus the value represented by the most significant bit of the upper value.

13. The CAM device of claim 1 wherein the lower value comprises a plurality of bits ordered from a most significant bit to a least significant bit, and wherein each of the plurality of compare circuits is adapted to store a respective one of the plurality of bits and to compare the one of the plurality of bits to a respective bit within the first comparand value.

14. The CAM device of claim 13 further comprising a match line and wherein a most significant compare circuit of the plurality of compare circuits is coupled to the match line, the most significant compare circuit including circuitry to affect a logical state of the match line if either (1) a most significant bit of the first comparand value is less than the most significant bit of the lower value, or (2) the most significant bit of the first comparand is equal to the most significant bit of the lower value, and a result signal from a less significant compare circuit of the plurality of compare circuits indicates that the first comparand value minus the value represented by the most significant bit of the first comparand value is less than the lower value minus the value represented by the most significant bit of the lower value.

15. A content addressable memory (CAM) cell comprising:

a first storage circuit to store a first boundary value; and

a first compare circuit to compare a comparand value to the first boundary value, the first compare circuit including circuitry to output a first result signal in a first state if the comparand value is greater than the first boundary value and in a second state if the comparand value is less than the first boundary value.

16. The CAM cell of claim 15 further comprising an input to receive a second result signal from another CAM cell, and wherein the circuitry to output the first result signal in the first state is adapted to output the first result signal in the first state if the comparand value is equal to the first boundary value and the second result signal is in the first state.

17. The CAM cell of claim 16 wherein the circuitry to output the first result signal is further adapted to output the first result signal in the second state if the comparand value is equal to the first boundary value and the second result signal is in the second state.

18. The CAM cell of claim 15 further comprising:

a second storage circuit to store a second boundary value; and

a second compare circuit to compare the comparand value to the second boundary value, the second compare circuit including circuitry to output a second result signal in the first state if the comparand is less than the second boundary value and in the second state if the comparand is greater than the second boundary value.

19. The CAM cell of claim 18 further comprising an input to receive a third result signal from a less significant CAM cell, and wherein the circuitry to output the second result signal in the first state is further adapted to output the second result signal in the first state if the comparand value is equal to the second boundary value and the third result signal is in the

first state.

20. The CAM cell of claim 15 wherein the circuitry to output the first result signal is adapted to output the first result signal in the first state if the comparand is equal to the first boundary value.

21. The CAM cell of claim 15 wherein the circuitry to output the first result signal is adapted to output the first result signal in the second state if the comparand is equal to the first boundary value.

22. The CAM cell of claim 15 wherein the first boundary value is an upper boundary value.

23. A content addressable memory (CAM) device comprising:

a first storage circuit to store a first value; and

a compare circuit coupled to the first storage circuit to receive the first value and coupled to a mode signal line to receive a mode signal, the compare circuit being adapted to compare a comparand value to the first value and to output a first result signal, the first result signal indicating whether the comparand value is greater than the first value when the mode signal is in a first state, and the first result signal indicating whether the comparand is equal to the first value when the mode signal is in a second state.

24. The CAM device of claim 23 further comprising a second storage circuit to store a second value and coupled to provide the second value to the compare circuit, the compare circuit including circuitry to compare the comparand value to the second value and to output a second result signal, the second result signal indicating whether the comparand is less than

the second value when the mode signal is in the first state.

25. The CAM device of claim 23 further comprising:

a second storage circuit to store a second value and coupled to provide the second value to the compare circuit, the compare circuit including circuitry to compare the comparand value to the second value and, when the mode signal is in the first state, to output a second result signal indicating whether the comparand is less than the second value; and

a mask circuit coupled to receive the second value from the storage circuit and coupled to the compare circuit, the mask circuit being adapted to selectively mask the first result signal, according to the second value, when the mode signal is in the second state.

26. The CAM device of claim 25 wherein the mask circuit is adapted to mask the first result signal by preventing the compare circuit from outputting the first result signal in a state indicative of inequality between the first value and the comparand.

27. The CAM device of claim 25 wherein the mask circuit is adapted to mask the first result signal by disabling the first value from being received in the compare circuit.

28. The CAM device of claim 25 wherein the mask circuit is adapted to mask the first result signal by disabling the comparand value from being received in the compare circuit.

29. A content addressable memory (CAM) device comprising:

a first storage circuit to store a first value; and

a first compare circuit coupled to receive the first value from the first storage circuit and having a select input to receive a level select signal, the first compare circuit being

adapted to compare a comparand value to the first value and to assert a beyond-boundary signal if the level select signal is in a first state and if the comparand value is greater than the first value, the first compare circuit being further adapted to assert the beyond-boundary signal if the level select signal is in a second state and if the comparand value is less than the first value.

30. The CAM device of claim 29 further comprising:

an first input to receive a first signal representative of the comparand value;

a second input to receive a second signal representative of a complement of the comparand value; and

a select circuit coupled to the first input and the second input to select, according to a state of the level select signal, either the first signal or the second signal to be output to the compare circuit for comparison with the first value.

31. The CAM device of claim 30 wherein the select circuit is a multiplexer having a control input coupled to receive the level select signal and having first and second ports coupled respectively to the first and second inputs.

32. The CAM device of claim 29 wherein the first value is representative of an upper boundary value when the level select signal is in the first state, and wherein the first value is representative of a lower boundary value when the level select signal is in the second state

33. The CAM device of claim 29 further comprising a mode select input to receive a mode select signal, the first compare circuit being enabled to assert the beyond-boundary signal if the mode select signal is in a first state and the first compare circuit being disabled from

asserting the beyond-boundary signal if the mode select signal is in a second state.

34. The CAM device of claim 33 further comprising a second compare circuit to compare the comparand value and the first value and to assert a match signal indicative of whether the comparand value is equal to the first value, the second compare circuit being enabled to assert the match signal if the mode select signal is in the second state, and the second compare circuit being disabled from asserting the match signal if the mode select signal is in the first state.

35. A content addressable memory (CAM) device comprising:

a CAM array having a plurality of CAM cells; and

at least one mode select line coupled to at least one set of CAM cells within the plurality of CAM cells, the set of CAM cells being adapted to compare a comparand value to a range defined by at least one boundary value stored within the set of CAM cells if a mode select signal on the mode select line is in a first state, and the set of CAM cells being adapted to compare the comparand value for equality with a data value stored within the set of CAM cells if the mode select signal is in a second state.

36. The CAM device of claim 35 further comprising a mode configuration circuit coupled to the mode select line, the mode configuration circuit including a storage circuit to store a mode value, the mode select signal being in either the first state or the second state according to the mode value.

37. The CAM device of claim 36 further comprising an interface to receive a first instruction from a host processor, the CAM device being adapted to store the mode value in the

storage circuit in response to the first instruction.

38. The CAM device of claim 36 further comprising a mode select interface, and wherein the mode select line is coupled to the mode select interface to receive the mode select signal from an external device.

39. The CAM device of claim 38 wherein the external device is a host processor.

40. A system comprising:

a processor; and

a content addressable memory (CAM) device coupled to receive instructions and data values from the processor, the CAM device including a plurality of CAM cells and being responsive to a first instruction from the processor to select either a first operating mode or a second operating mode for the plurality of CAM cells, the plurality of CAM cells being adapted to compare a comparand value to a range defined by at least one boundary value stored within the plurality of CAM cells if the first operating mode is selected, and the plurality of CAM cells being adapted to compare the comparand value for equality with a data value stored within the plurality of CAM cells if the second operating mode is selected.

41. The system of claim 40 wherein the CAM device includes a mode configuration circuit to store a mode select value in response to the first instruction, the mode select value indicating the first operating mode or the second operating mode according to the first instruction.

42. The system of claim 41 wherein the plurality of CAM cells is responsive to the mode select

value to operate in either the first operating mode or the second operating mode.

43. The system of claim 41 wherein the CAM device includes additional CAM cells configured to operate only in the second operating mode.

44. The system of claim 41 wherein the CAM device includes additional CAM cells configured to operate only in the second operating mode.

45. A system comprising:

a processor; and

a content addressable memory (CAM) device coupled to receive instructions from the processor, the CAM device including a first plurality of CAM cells and being responsive to a first instruction from the processor to store a first boundary value in the first plurality of CAM cells, the first plurality of CAM cells being adapted to compare the first boundary value with a first comparand value in a compare operation and to output a first result signal indicative of whether the first comparand value is greater than the first boundary value.

46. The system of claim 45 wherein the first plurality of CAM cells are responsive to a mode select signal to operate in either a range mode or a ternary mode, the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode.

47. The system of claim 45 wherein the first plurality of CAM cells are responsive to a mode select signal to operate in either a range mode or a binary mode, the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode.

48. They system of claim 45 wherein the CAM device further includes a second plurality of CAM cells to store a data value, the second plurality of CAM cells being adapted to compare the data value with a second comparand value in a compare operation and to output a first result signal indicative of whether the second comparand value is equal to the data value.

49. The system of claim 48 wherein the first plurality of CAM cells and the second plurality of CAM cells are each included within a first row of CAM cells within the CAM device.

50. The system of claim 48 wherein the first comparand value and the second comparand value each constitute a respective field of bits within a third comparand value.

51. The system of claim 45 wherein the CAM device is further responsive to the first instruction from the processor to store a second boundary value in the first plurality of CAM cells, and the first plurality of CAM cells being further adapted to compare the second boundary value with the second comparand in the compare operation and to output a second result signal indicative of whether the first comparand value is less than the second boundary value.

52. The system of claim 45 wherein the CAM device includes multiple independently searchable storage blocks each including a plurality of CAM cells therein, the first plurality of claim cells being included within the plurality of CAM cells in one of the searchable storage blocks.

53. The system of claim 52 wherein the CAM device further includes a block configuration

circuit to store a block configuration value, and circuitry to configure at least one of the storage blocks to have a storage width and depth according to the block configuration value.

54. The system of claim 53 wherein the CAM device is responsive to a second instruction from the processor to store the block configuration value in the block configuration circuit.

55. The system of claim 53 wherein the block configuration circuit is adapted to store a mode value, and wherein the first plurality of CAM cells are responsive to the mode value to operate in either a range mode or a ternary mode, the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode.

56. The system of claim 55 wherein the CAM device is responsive to a second instruction from the processor to store the mode value in the block configuration circuit.

57. The system of claim 53 wherein the block configuration circuit is adapted to store a mode value, and wherein the first plurality of CAM cells are responsive to the mode value to operate in either a range mode or a binary mode, the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode.

58. A method of operation within a content addressable memory (CAM) device, the method comprising:

comparing a comparand value with a first boundary value stored in a plurality of CAM cells within the CAM device; and

asserting a first result signal if the comparand value is greater than the first boundary value.

59. The method of claim 58 further comprising storing the first boundary value in the plurality of CAM cells in response to a write instruction.

60. The method of claim 58 wherein comparing the comparand value with the first boundary value comprises, in each CAM cell of the plurality of CAM cells, asserting a greater-than signal if either (1) a bit of the comparand value received within the CAM cell is greater than a bit of the first boundary value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit of the first boundary value and a greater-than signal is received from a less significant CAM cell within the plurality of CAM cells.

61. The method of claim 61 wherein a greater-than signal asserted by a most significant one of the plurality of CAM cells constitutes the first result signal.

62. The method of claim 58 further comprising:

comparing a comparand value with a second boundary value stored in the plurality of CAM cells; and

asserting a second result signal if the comparand value is less than the second boundary value.

63. The method of claim 62 wherein comparing the comparand value with the second boundary value comprises, in each CAM cell of the plurality of CAM cells, asserting a less-than signal if either (1) a bit of the comparand value received within the CAM cell is less than a bit of the second boundary value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit of the second boundary value and a less-than signal is received from a less significant CAM cell within the plurality of CAM cells.

64. The method of claim 63 wherein a less-than signal asserted by a most significant one of the plurality of CAM cells constitutes the second result signal.

65. A content addressable memory (CAM) device comprising:
means for comparing a comparand value with a first boundary value stored in a plurality of CAM cells within the CAM device; and
means for asserting a first result signal if the comparand value is greater than the first boundary value.

66. The CAM device of claim 65 further comprising means for storing the first boundary value in the plurality of CAM cells in response to a write instruction.

67. The CAM device of claim 65 wherein the means for comparing a comparand value with a first boundary value comprises respective means within each CAM cell of the plurality of CAM cells for asserting a greater-than signal if either (1) a bit of the comparand value received within the CAM cell is greater than a bit of the first boundary value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit of the first boundary value and a greater-than signal is received from a less significant CAM cell within the plurality of CAM cells.

68. The CAM device of claim 65 further comprising:
means for comparing a comparand value with a second boundary value stored in the plurality of CAM cells; and
means for asserting a second result signal if the comparand value is less than the second boundary value.

69. The CAM device of claim 68 wherein the means for comparing a comparand value with a second boundary value comprises respective means within each CAM cell of the plurality of CAM cells for asserting a less-than signal if either (1) a bit of the comparand value received within the CAM cell is less than a bit of the second boundary value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit of the second boundary value and a less-than signal is received from a less significant CAM cell within the plurality of CAM cells.